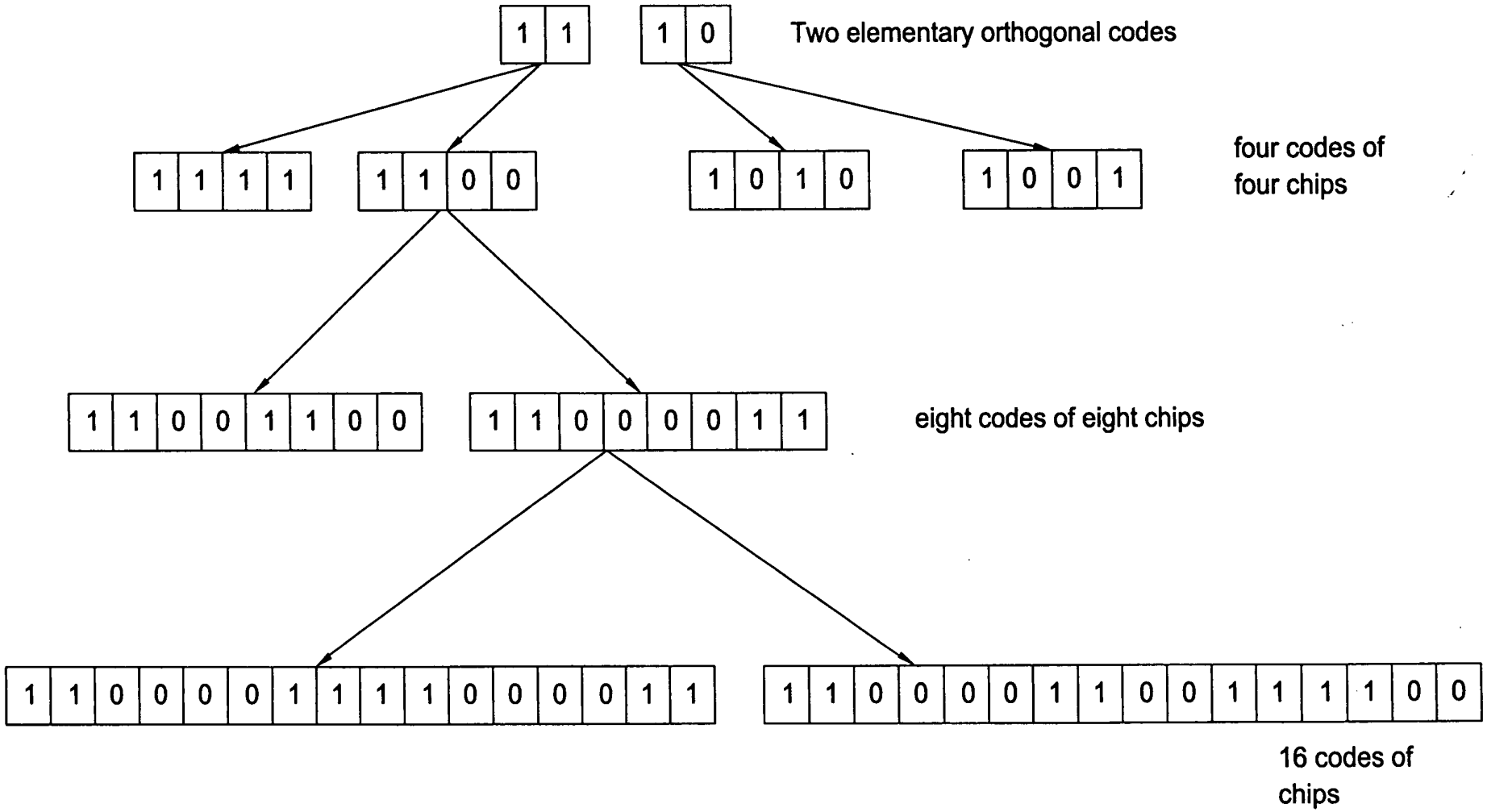
1 1
1 0
Two elementary orthogonal codes
1 1 1 1
1 1 0 0
1 0 1 0
1 0 0 1
four codes of four chips
1 1 0 0 1 1 0 0
1 1 0 0 0 0 1 1
eight codes of eight chips
1 1 0 0 0 0 1 1 1 1 0 0 0 0 1 1
1 1 0 0 0 0 1 1 0 0 1 1 1 1 0 0
16 codes of chips

FIG. 1.

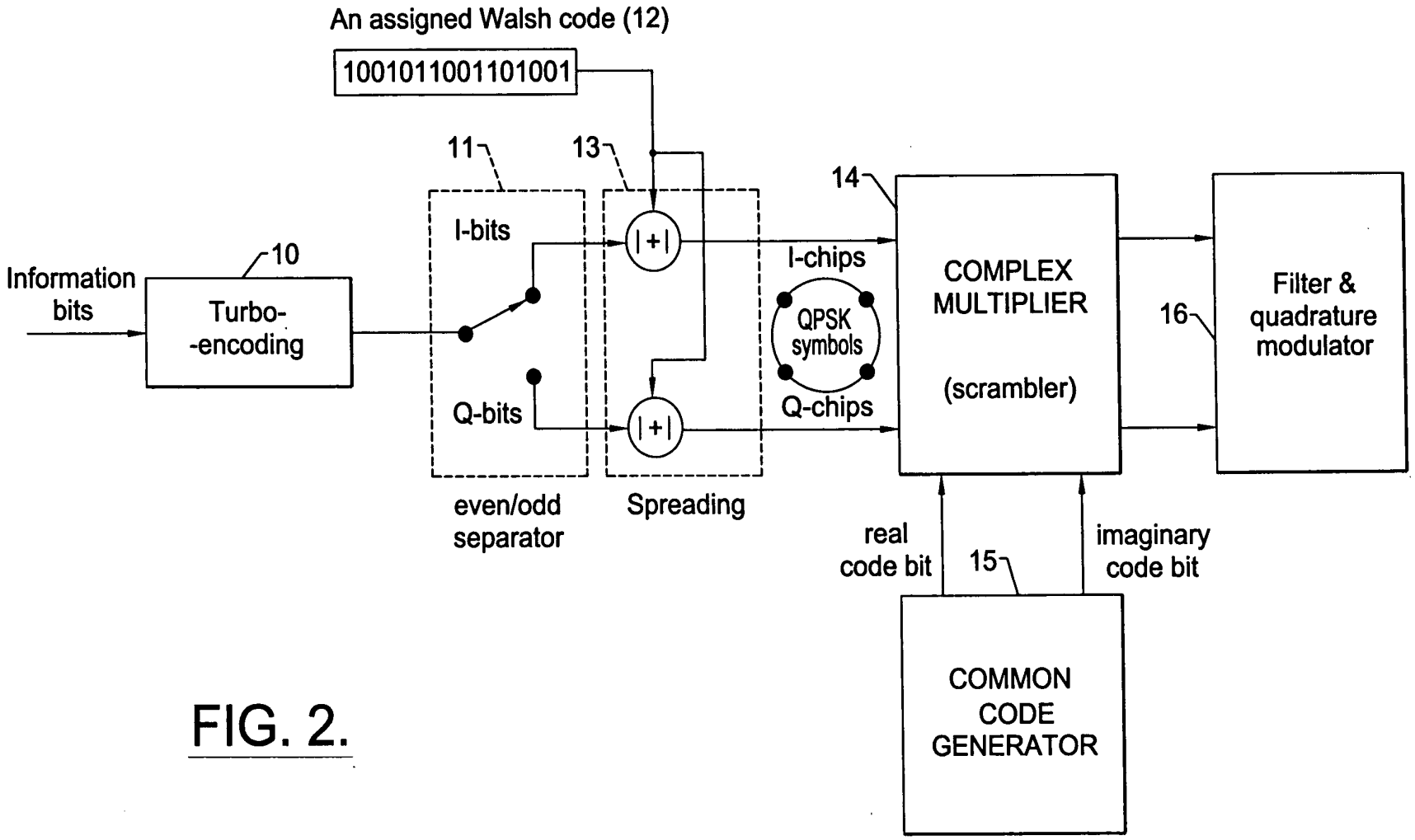

FIG. 2.

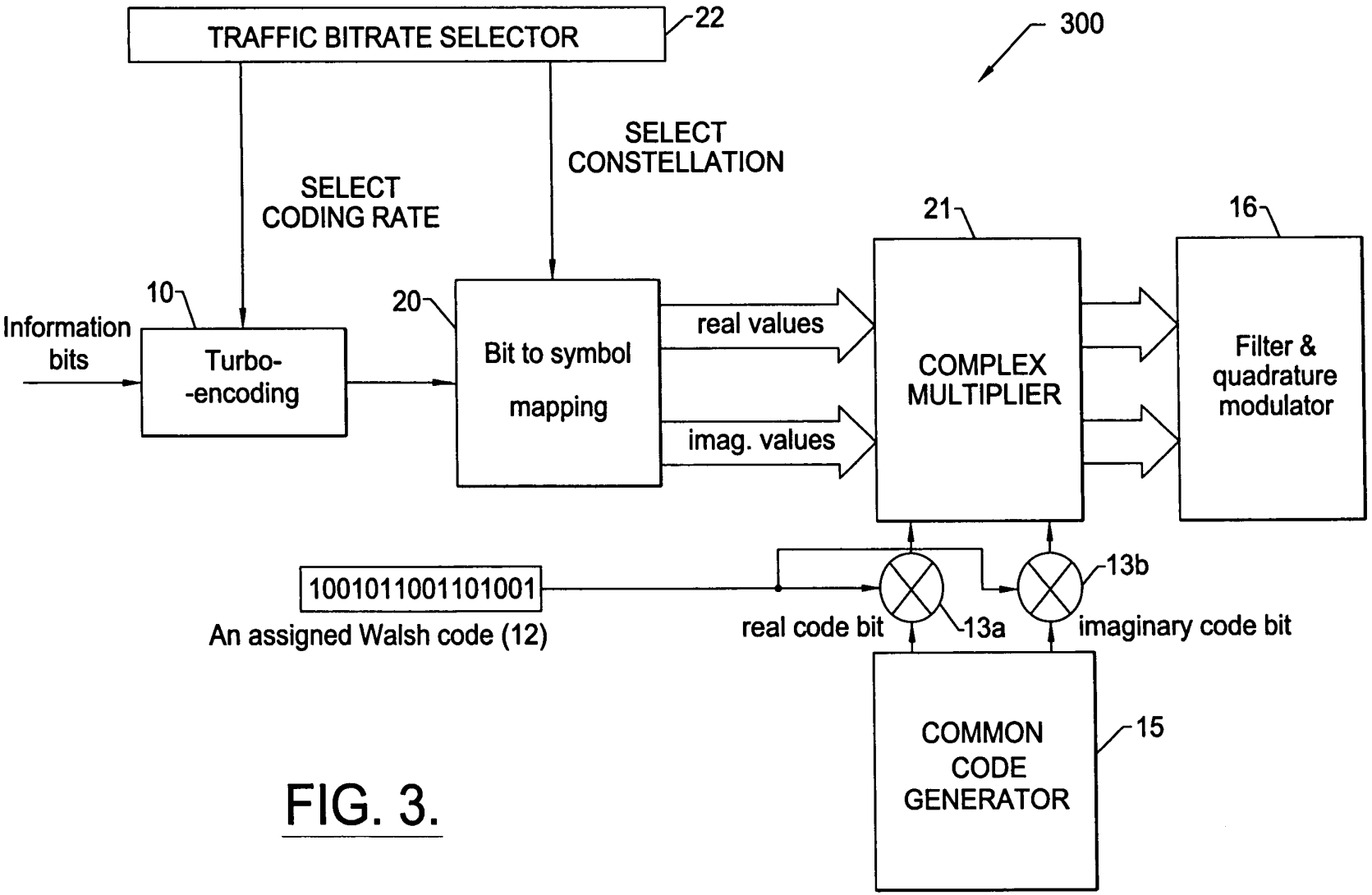
TRAFFIC BITRATE SELECTOR
22
300
SELECT CODING RATE
SELECT CONSTELLATION
21
16
10
20
Information bits
Turbo--encoding
Bit to symbol mapping
real values
imag. values
COMPLEX MULTIPLIER
Filter & quadrature modulator
13b
1001011001101001
An assigned Walsh code (12)
real code bit
13a
imaginary code bit
COMMON CODE GENERATOR
15

FIG. 3.

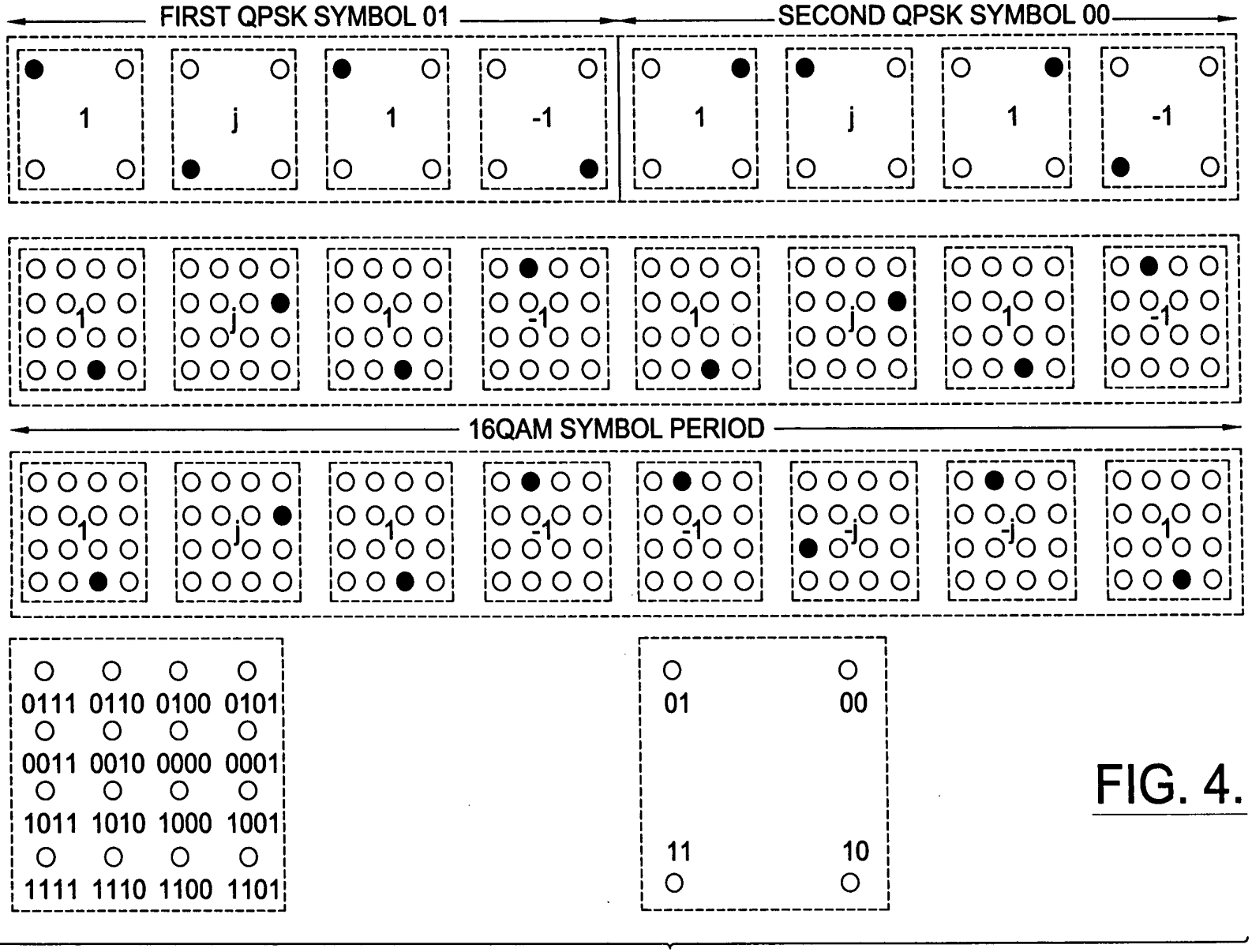

FIG. 4.

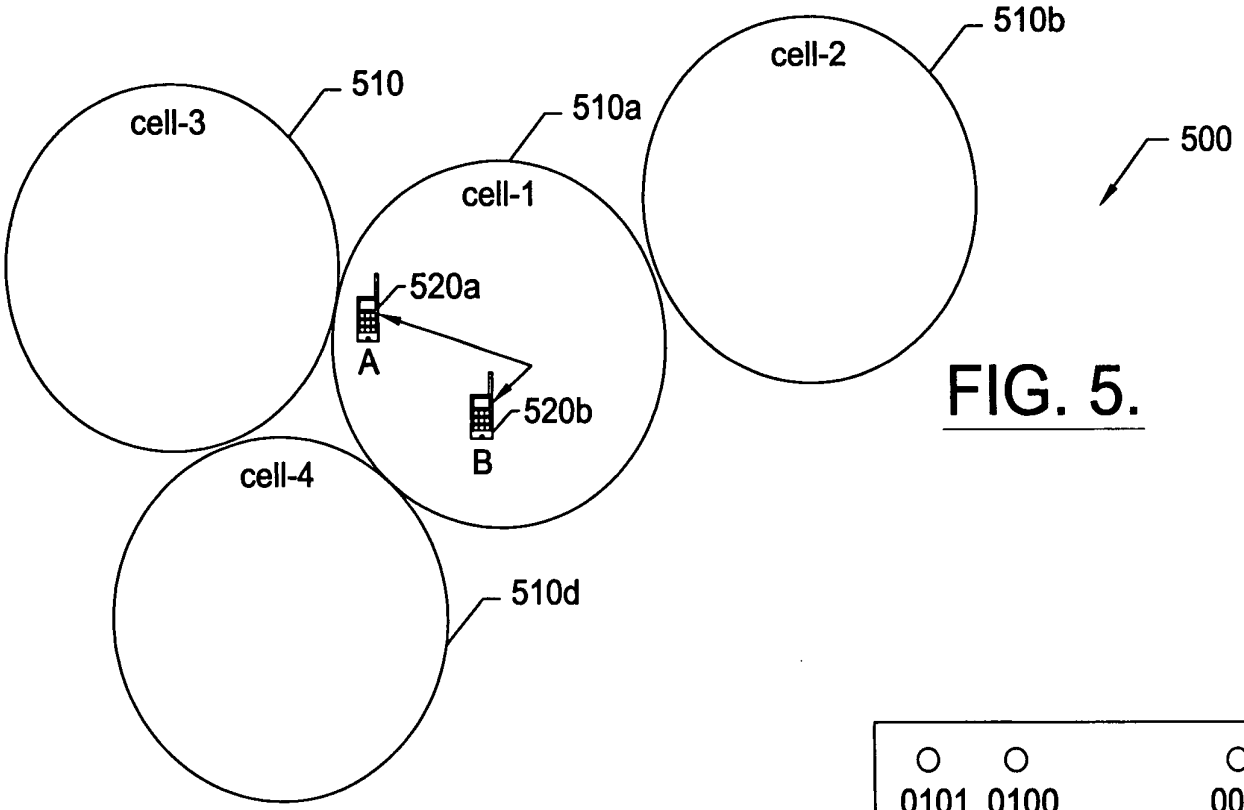

FIG. 5.

16QAM with non-equal power division between bit pairs

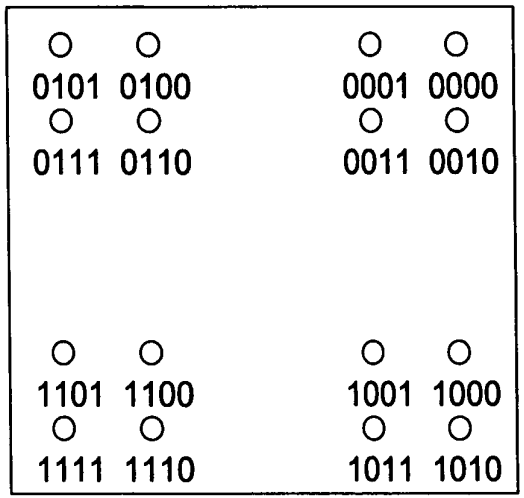

FIG. 6.

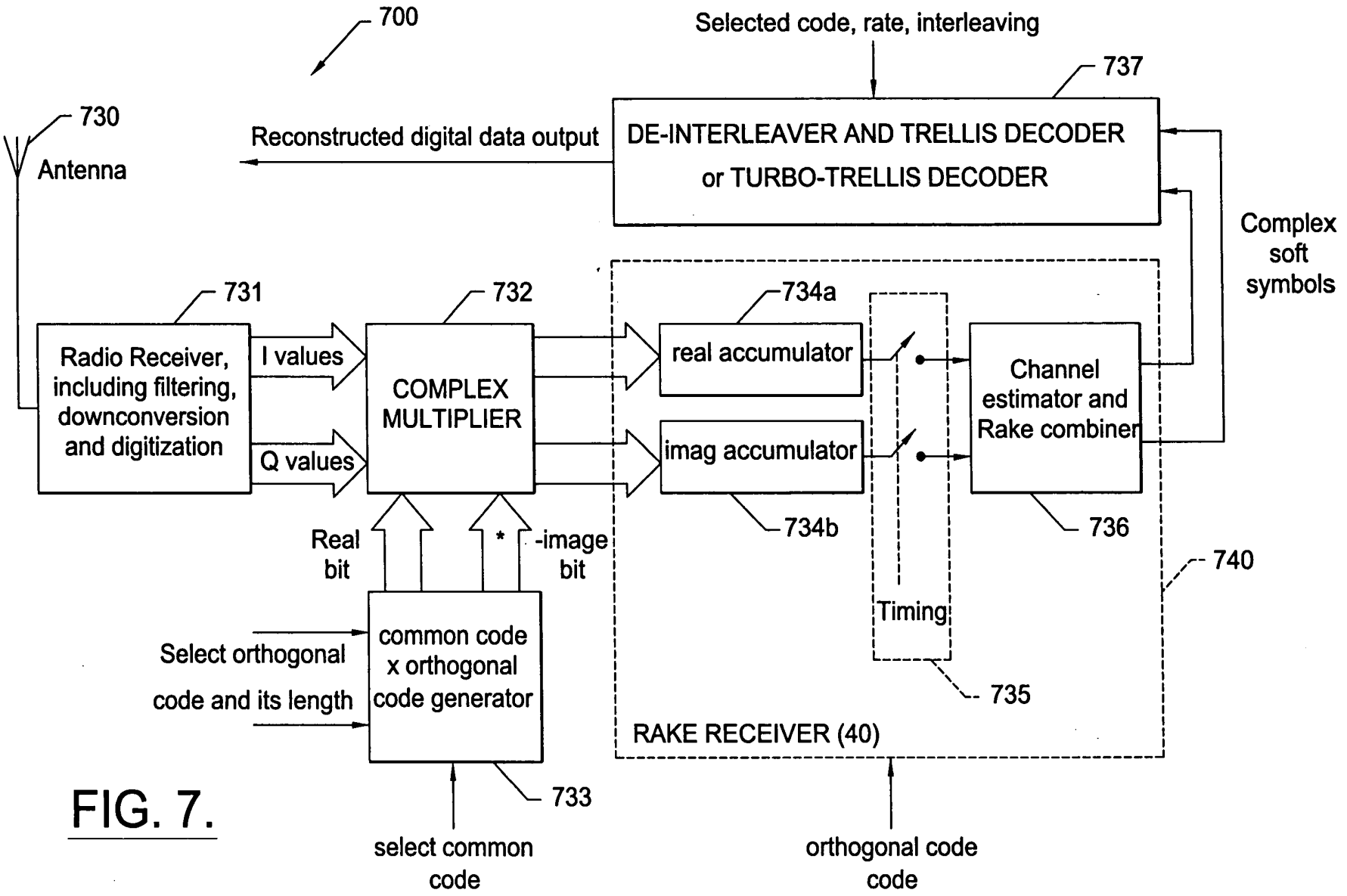

FIG. 7.

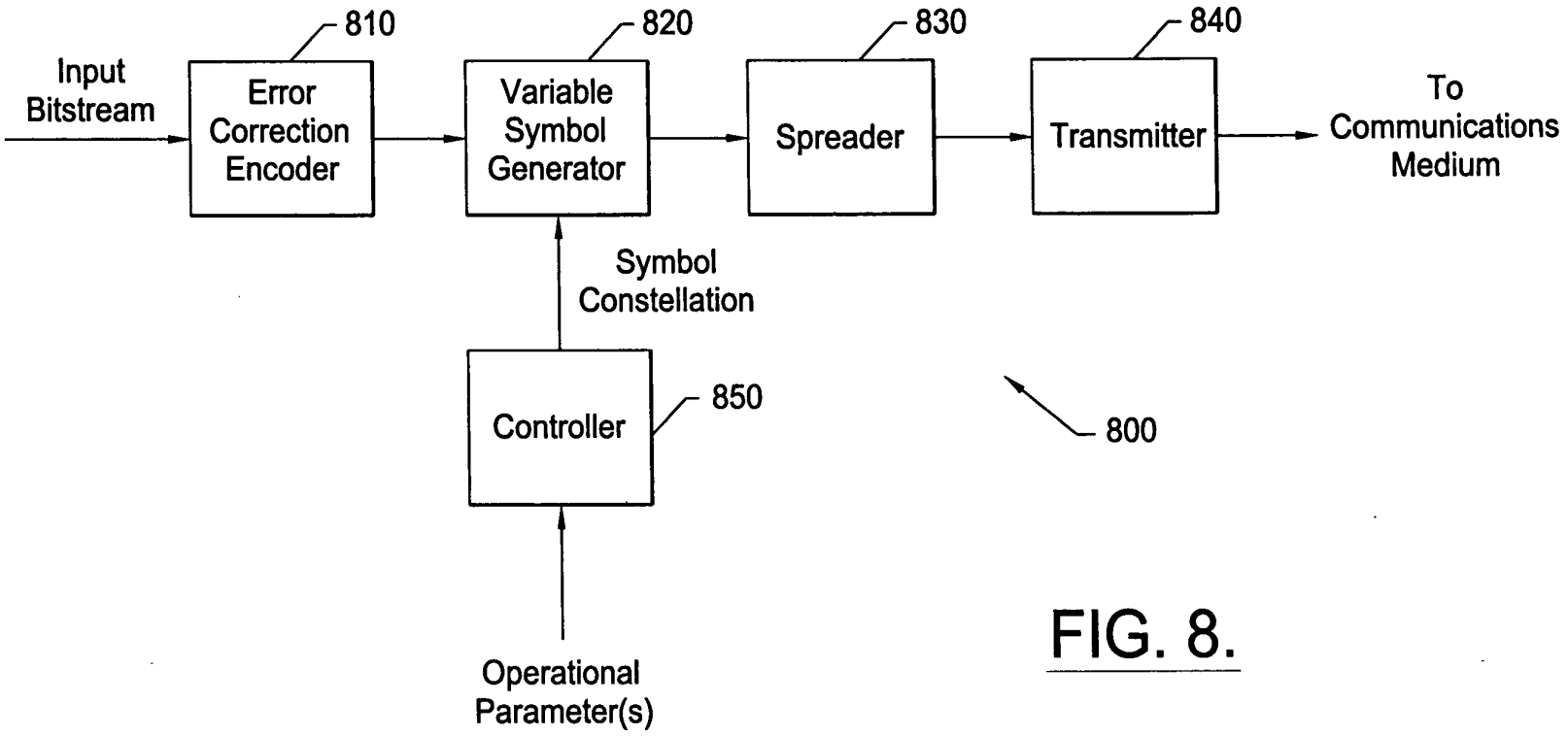

FIG. 8.

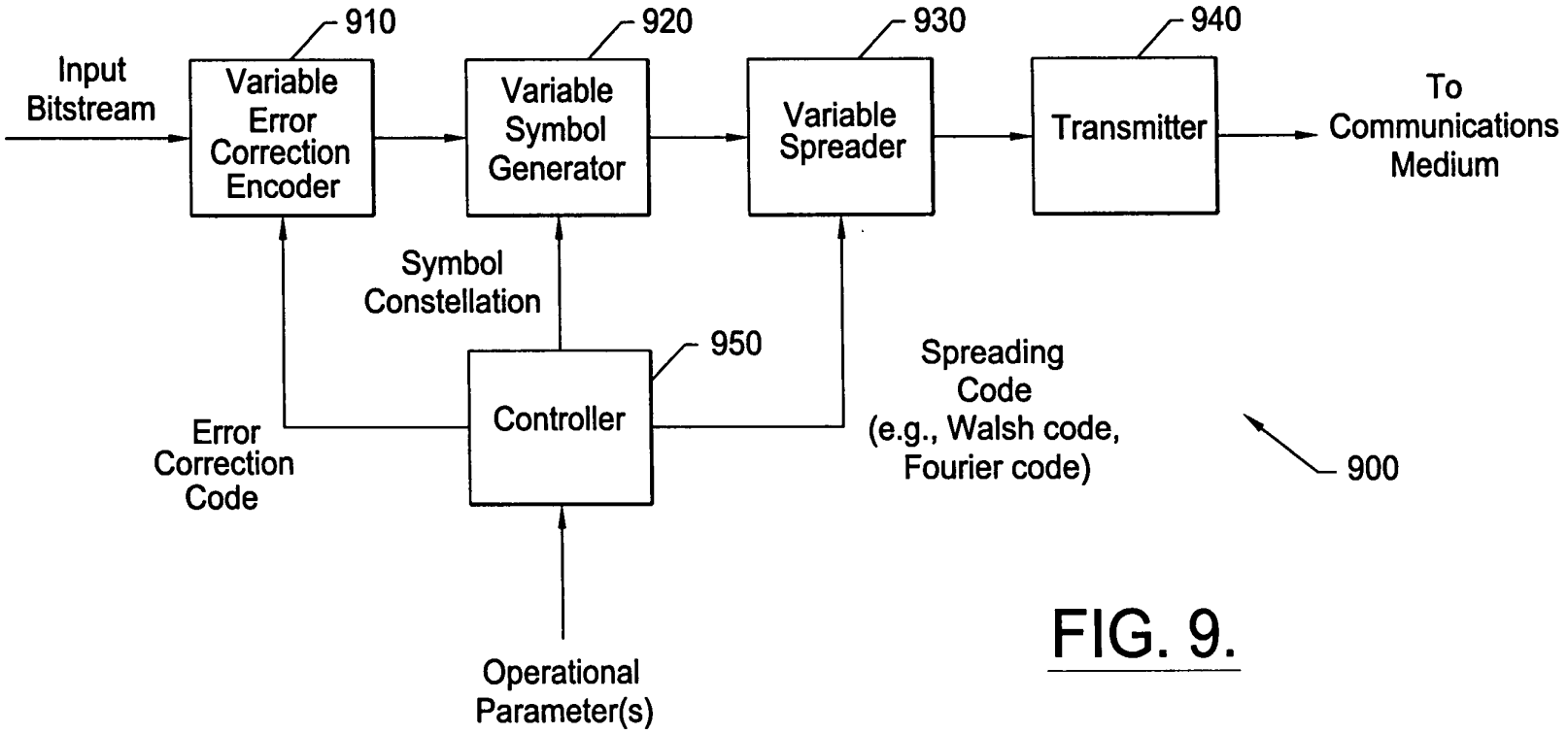
910
920
930
940
Input Bitstream
Variable Error Correction Encoder
Variable Symbol Generator
Variable Spreader
Transmitter
To Communications Medium
Symbol Constellation
950
Controller
Spreading Code (e.g., Walsh code, Fourier code)
900
Error Correction Code
Operational Parameter(s)

FIG. 9.

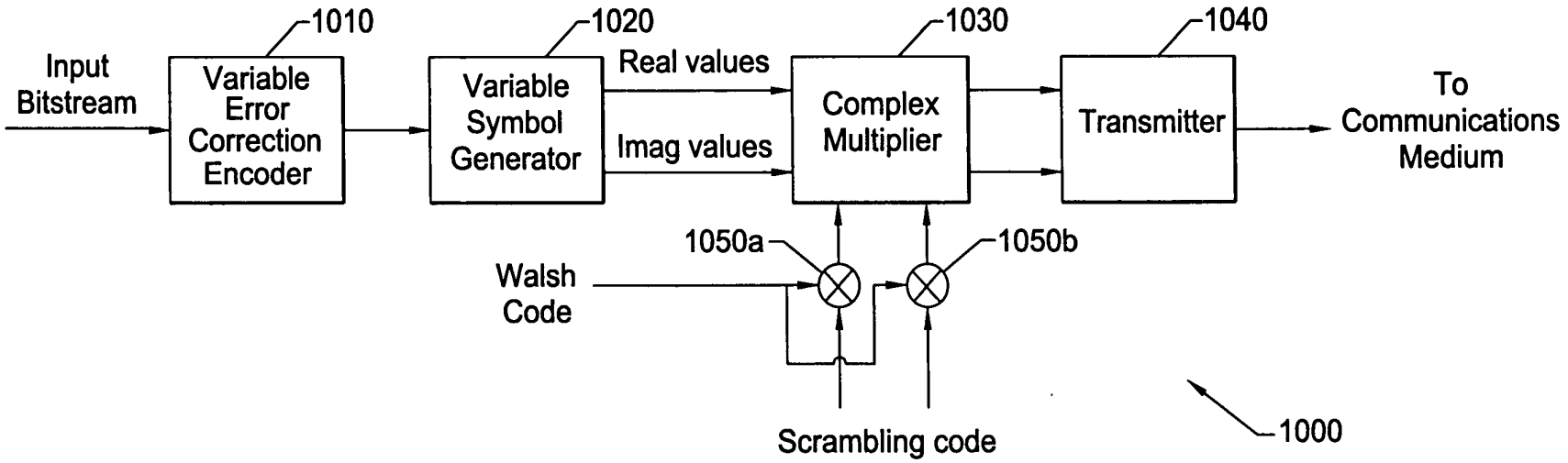
1010
1020
1030
1040
Input Bitstream
Variable Error Correction Encoder
Variable Symbol Generator
Real values
Imag values
Complex Multiplier
Transmitter
To Communications Medium
1050a
1050b
Walsh Code
Scrambling code
1000

FIG. 10.

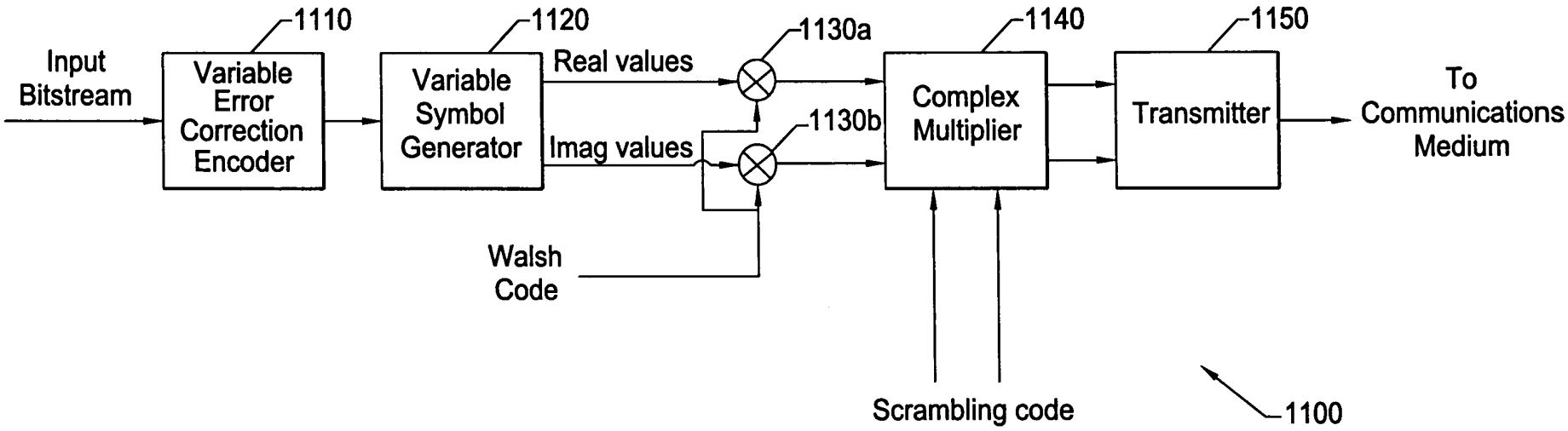
Input Bitstream
1110
Variable Error Correction Encoder
1120
Variable Symbol Generator
Real values
Imag values
1130a
1130b
Walsh Code
1140
Complex Multiplier
1150
Transmitter
To Communications Medium
Scrambling code
1100

FIG. 11.

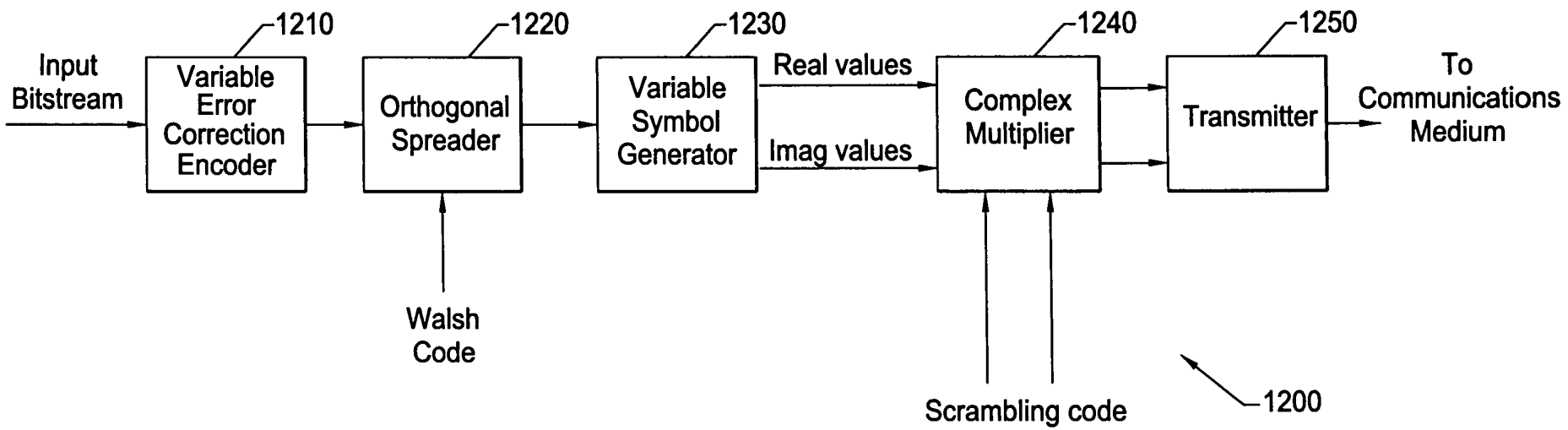

FIG. 12.

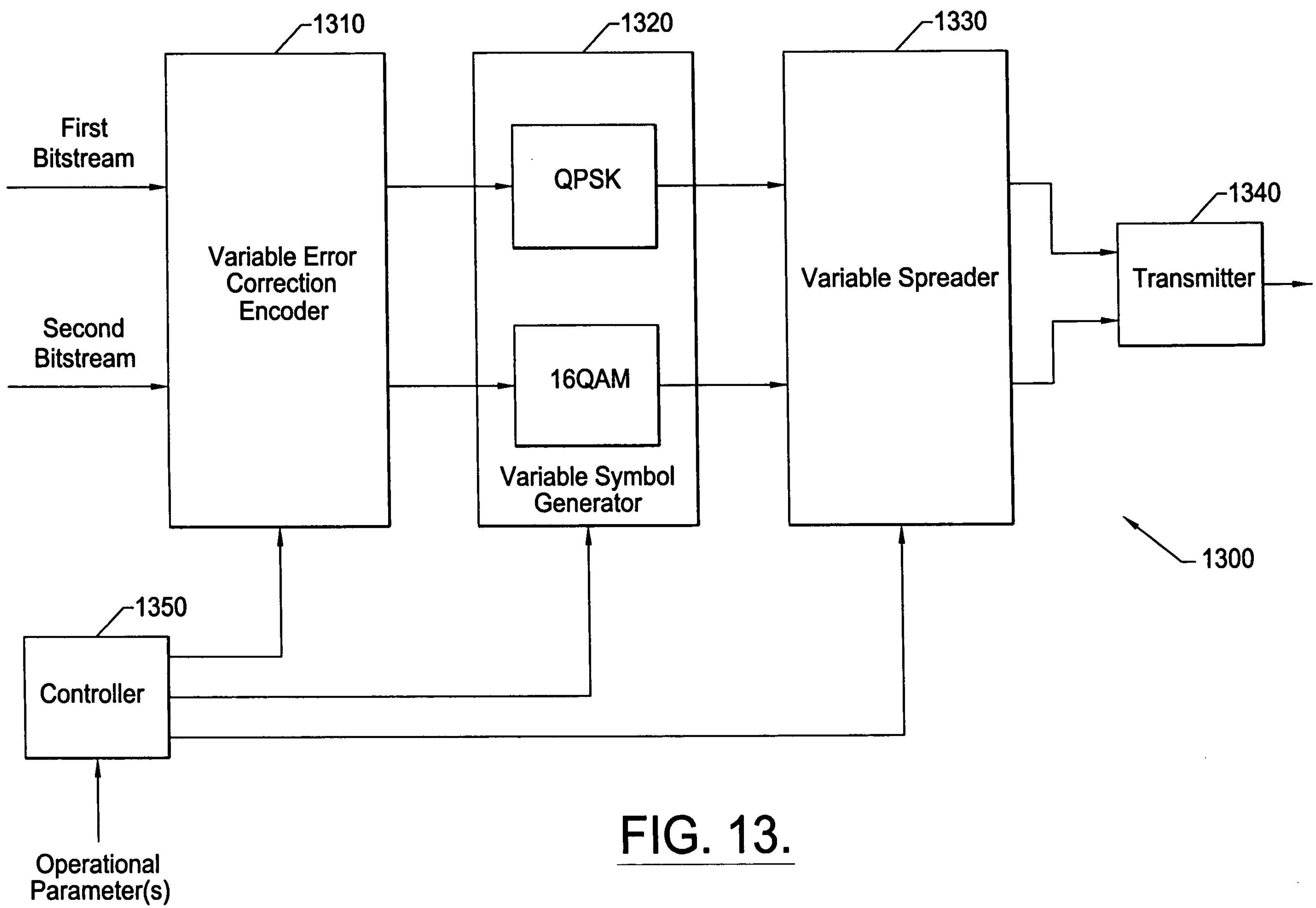
1310
1320
1330
1340
First Bitstream
Second Bitstream
Variable Error Correction Encoder
QPSK
16QAM
Variable Symbol Generator
Variable Spreader
Transmitter
1300
1350
Controller
Operational Parameter(s)

FIG. 13.

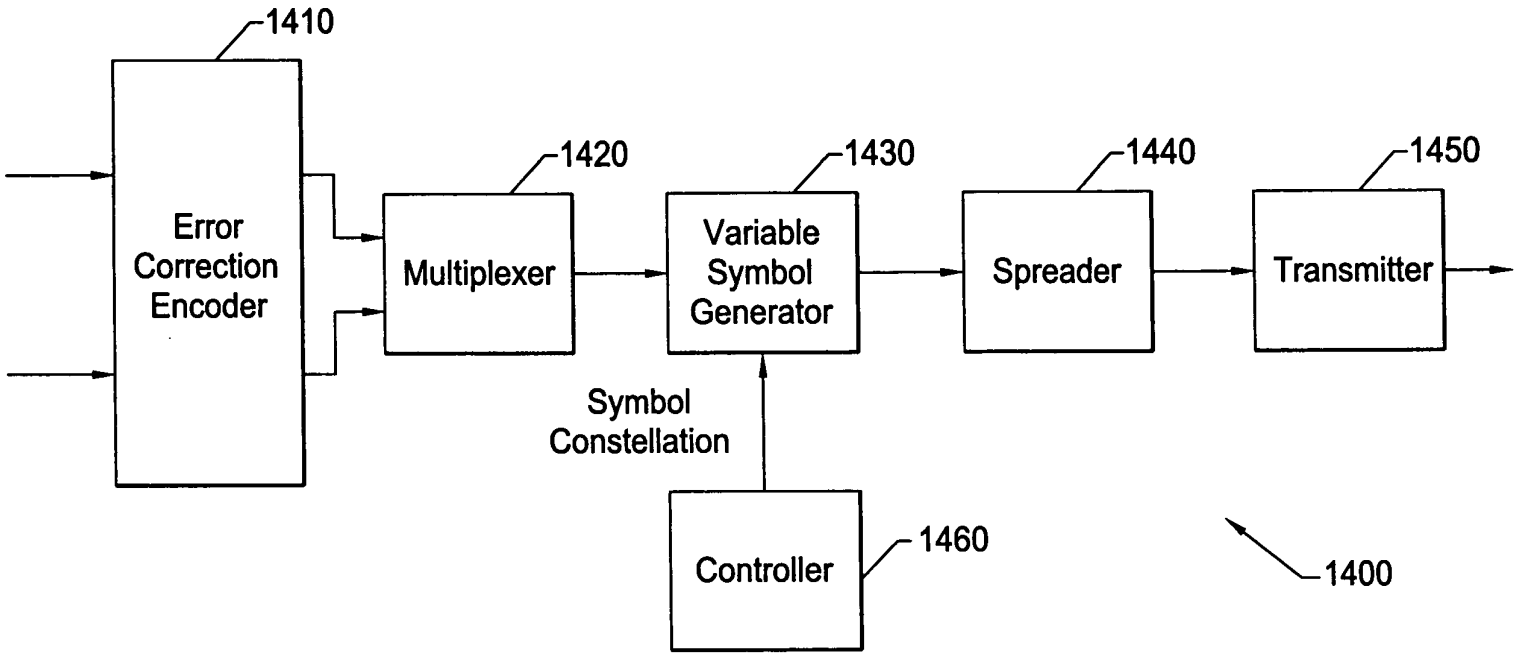

FIG. 14.

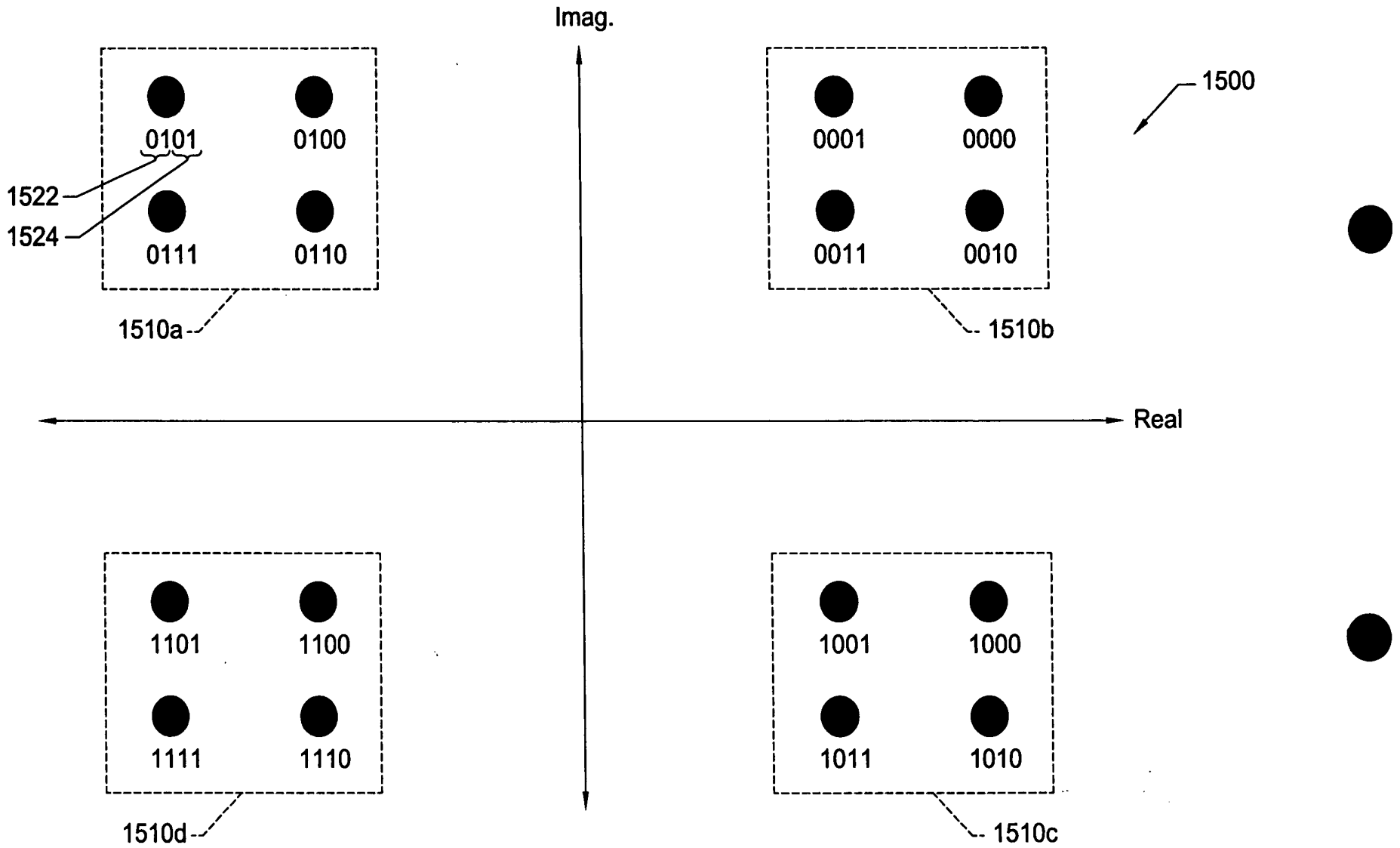
Imag.
Real
1500
0101
0100
0111
0110
1522
1524
1510a
0001
0000
0011
0010
1510b
1101
1100
1111
1110
1510d
1001
1000
1011
1010
1510c

FIG. 15.

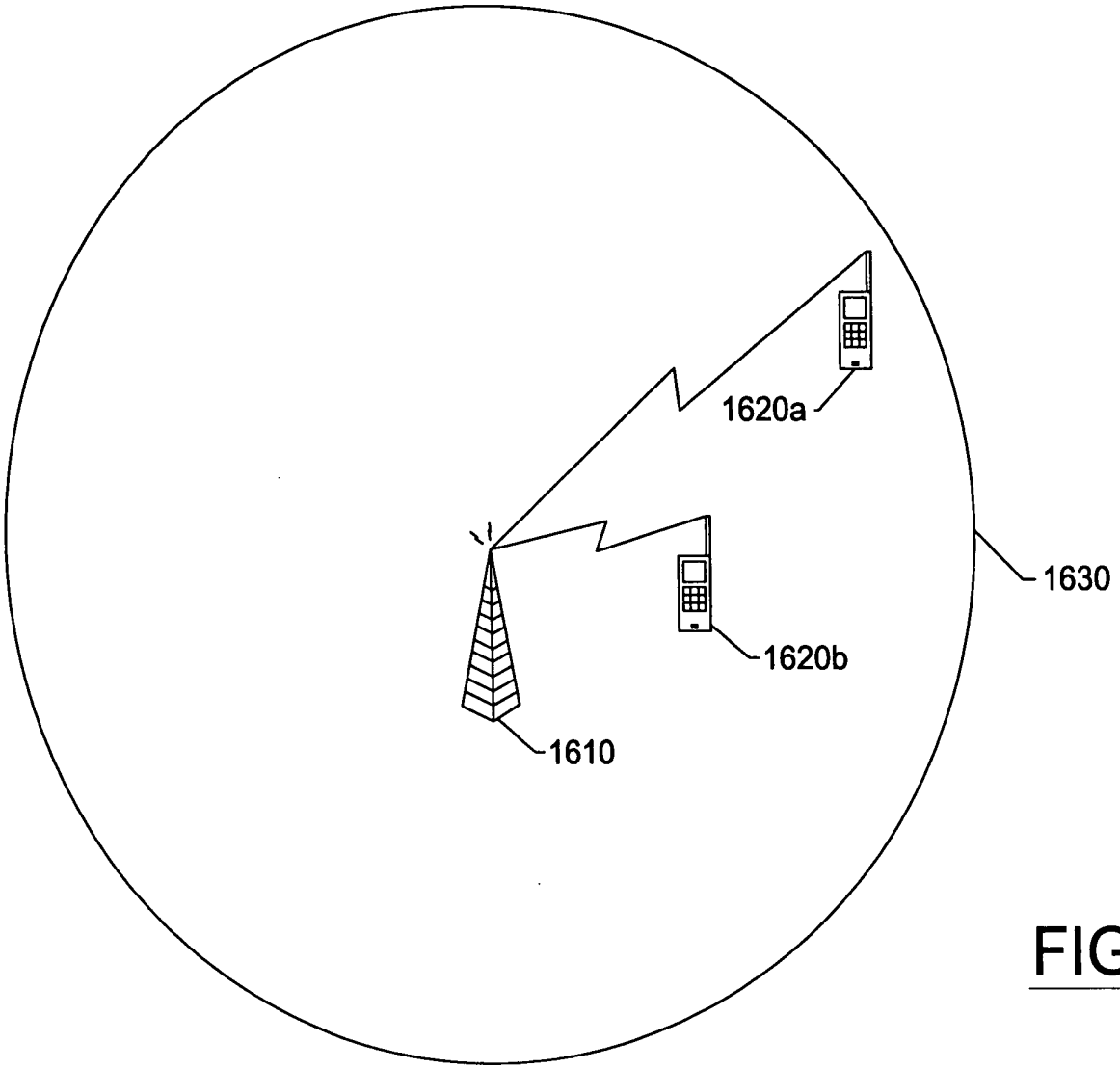

FIG. 16.

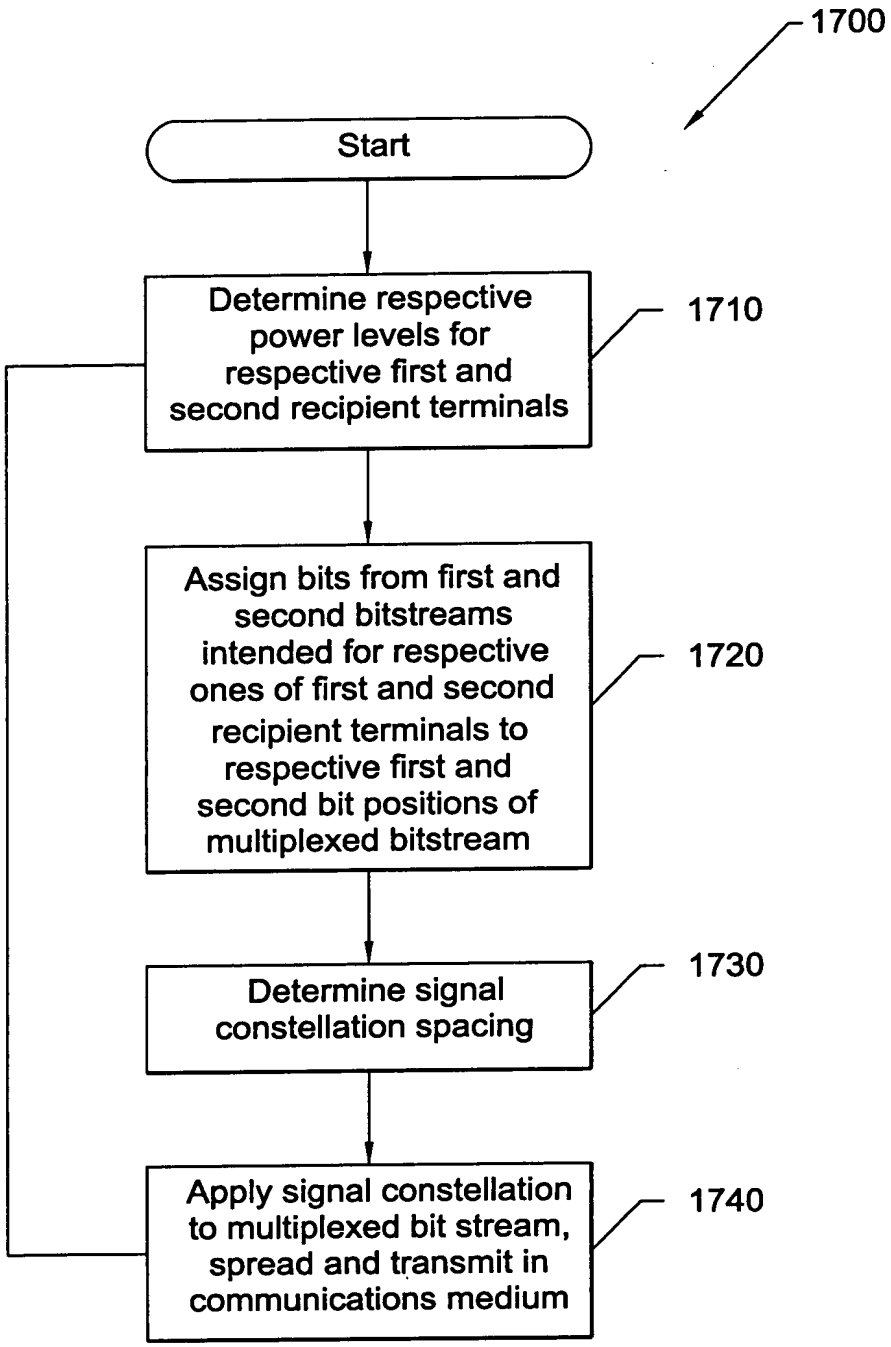
1700
Start
Determine respective power levels for respective first and second recipient terminals
1710
Assign bits from first and second bitstreams intended for respective ones of first and second recipient terminals to respective first and second bit positions of multiplexed bitstream
1720
Determine signal constellation spacing
1730
Apply signal constellation to multiplexed bit stream, spread and transmit in communications medium
1740

FIG. 17.

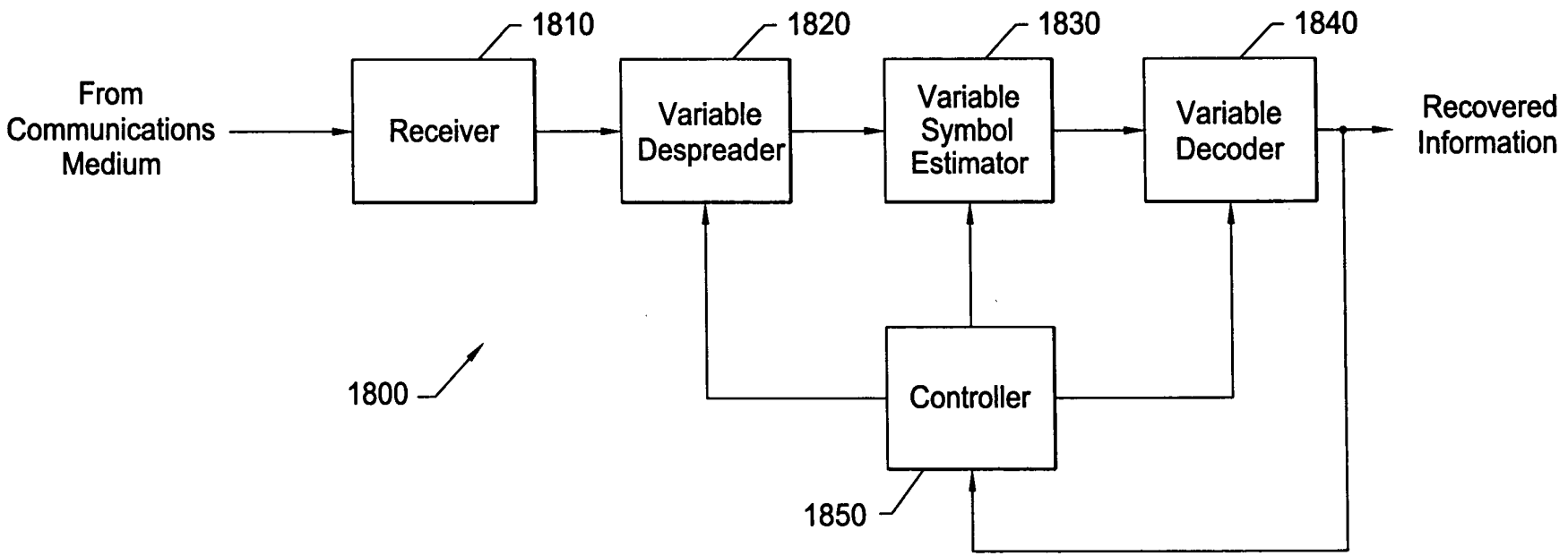

FIG. 18.

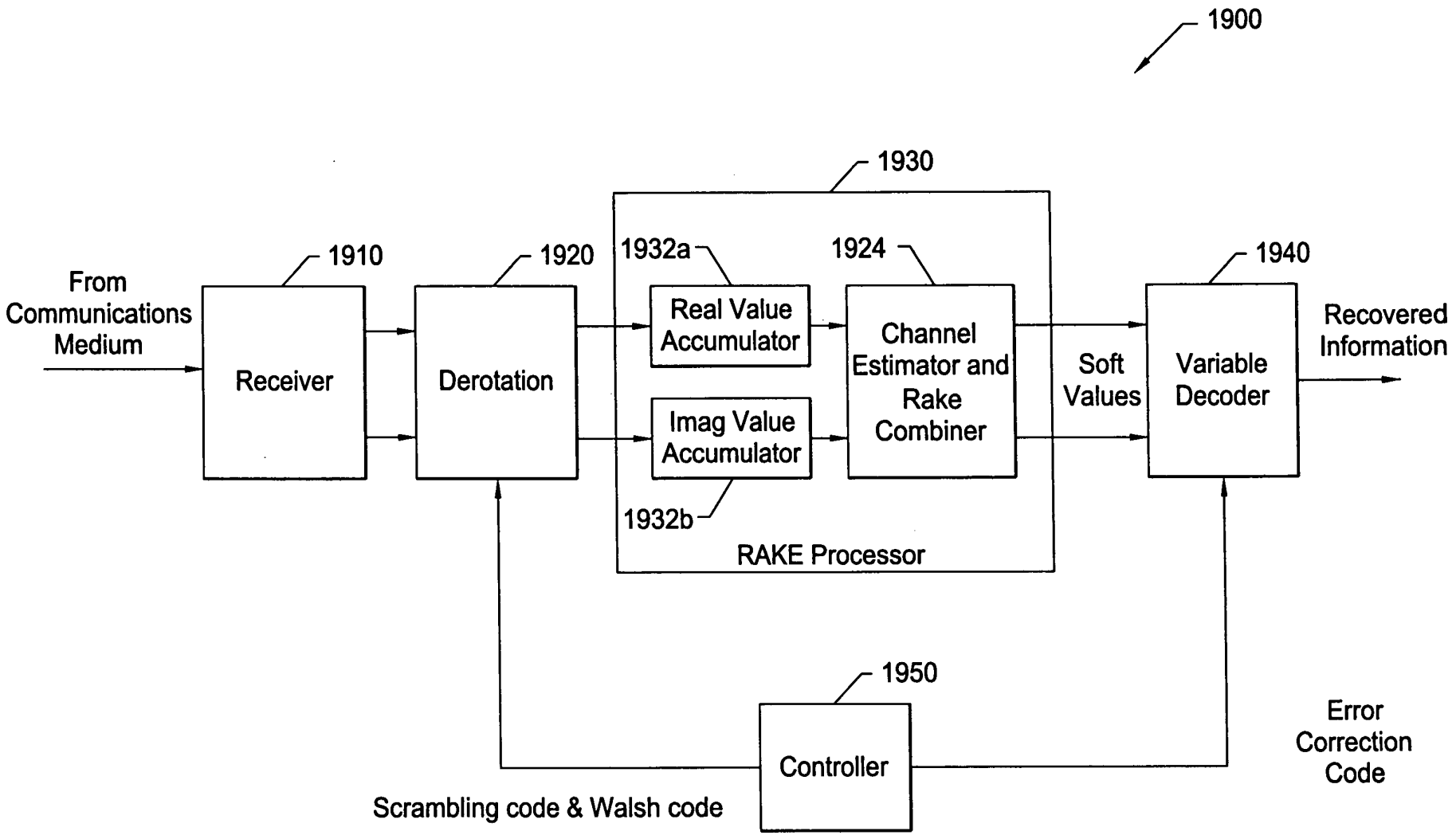
1900
1930
1910
1920
1932a
1924
1940
From Communications Medium
Receiver
Derotation
Real Value Accumulator
Channel Estimator and Rake Combiner
Soft Values
Variable Decoder
Recovered Information
Imag Value Accumulator
1932b
RAKE Processor
1950
Controller
Error Correction Code
Scrambling code & Walsh code

FIG. 19.

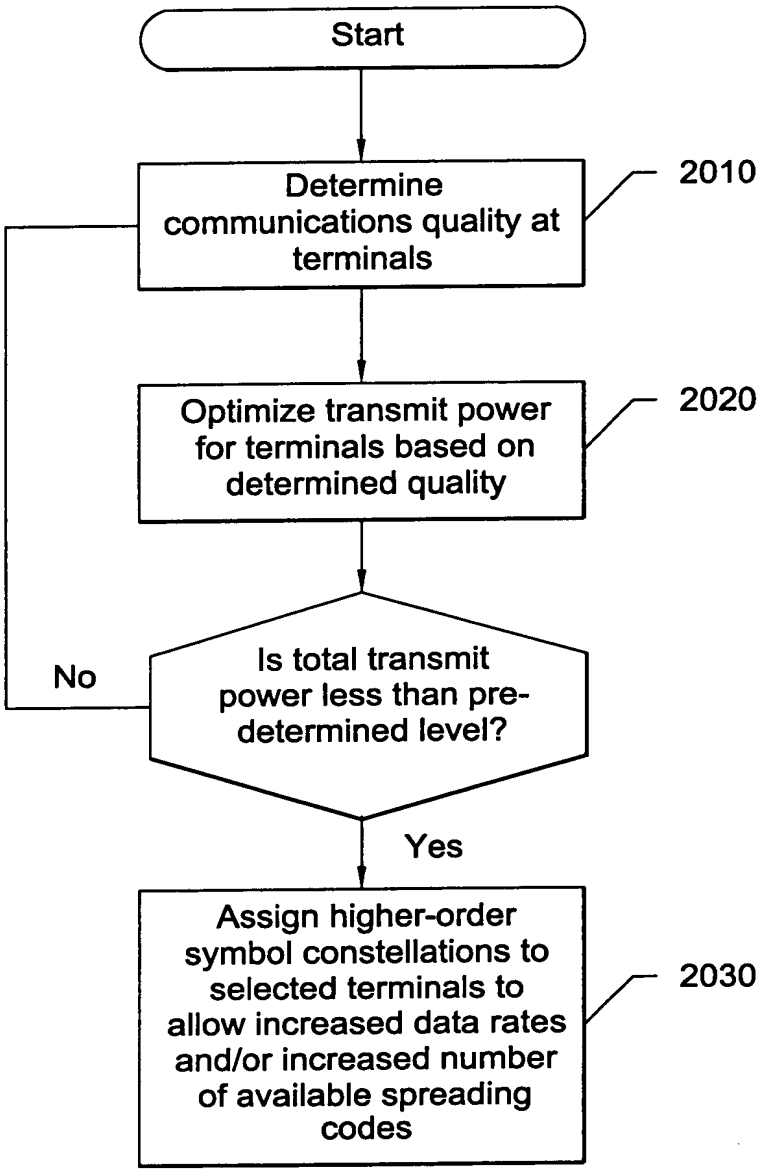

FIG. 20.

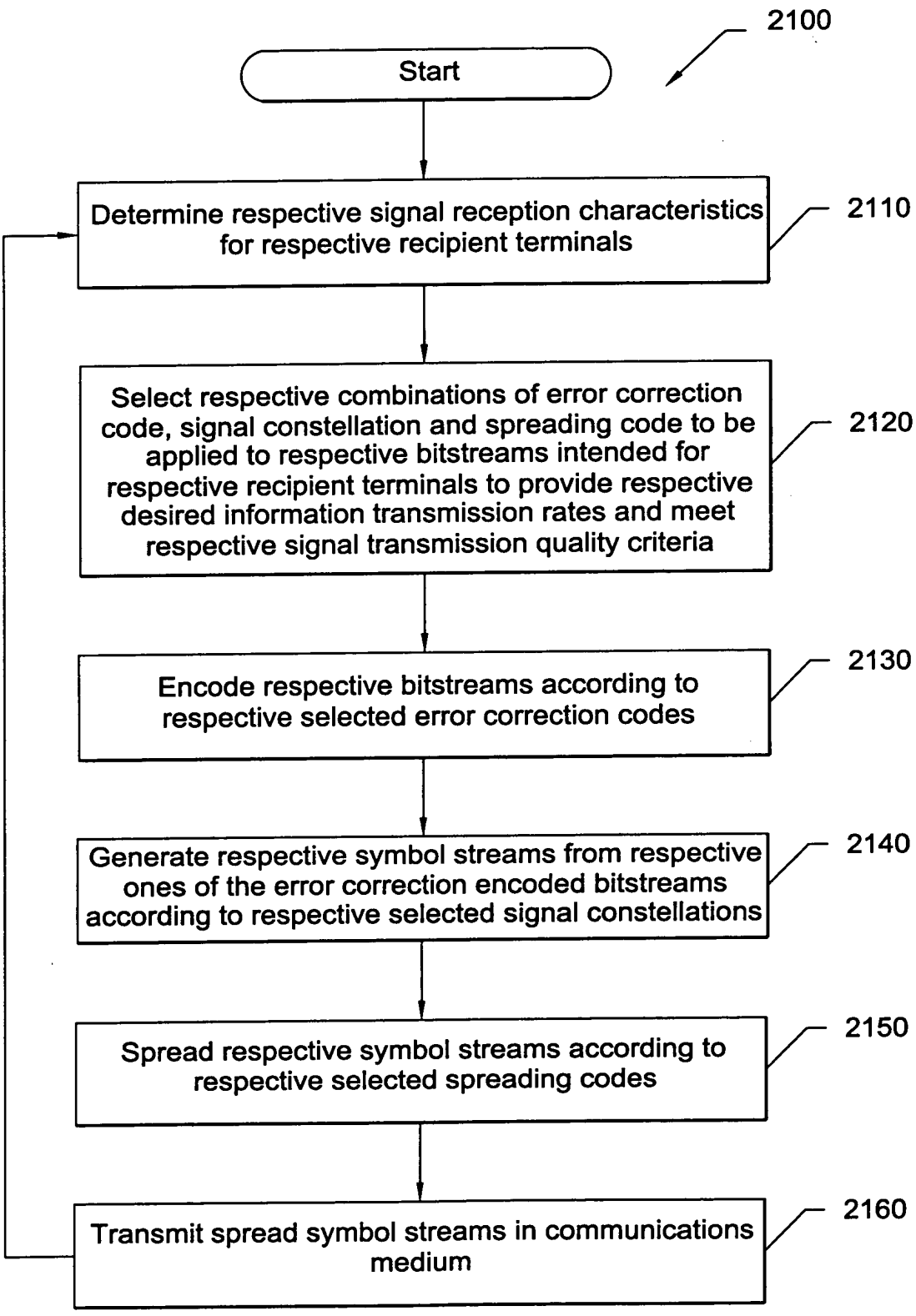
2100
Start
Determine respective signal reception characteristics for respective recipient terminals
2110
Select respective combinations of error correction code, signal constellation and spreading code to be applied to respective bitstreams intended for respective recipient terminals to provide respective desired information transmission rates and meet respective signal transmission quality criteria
2120
Encode respective bitstreams according to respective selected error correction codes
2130
Generate respective symbol streams from respective ones of the error correction encoded bitstreams according to respective selected signal constellations
2140
Spread respective symbol streams according to respective selected spreading codes
2150
Transmit spread symbol streams in communications medium
2160

FIG. 21.